Claims

What is claimed is:

1. A lead frame for packaging a semiconductor chip, the lead frame comprising:

a frame-shaped land;

a die pad for mounting the semiconductor chip;

first to fourth support portions formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and

first to fourth groups of lead members having first ends and second ends, the first ends being fixed to the land, and the second ends being parallel in each group.

2. A lead frame according to Claim 1, wherein the first to fourth groups of lead members are formed in first to fourth trapezoidal areas, the shorter bases of which face a center of the land and the longer bases of which face sides of the land, and the second ends of the first to fourth groups of lead members are along the shorter bases of the first to fourth trapezoidal areas.

3. A method for manufacturing a semiconductor device including a lead frame having a frame-shaped land; a die pad for mounting the semiconductor chip; first to fourth support portions formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and first to fourth groups of lead members having first ends and second ends, the first ends being fixed to the land, and the second ends being parallel in each group , the method comprising the steps of:

(a) cutting the first to fourth groups of lead members according to the size of the semiconductor chip to be packaged;

(b) mounting the semiconductor chip on the die pad;

(c) bonding the first to fourth groups of lead members and the semiconductor chip with a plurality of wires;

(d) fitting terminals to the land, for connecting the first to fourth groups of lead members to an external circuit; and

(e) encapsulating the lead frame and the semiconductor chip.

4. A package for packaging a semiconductor chip, the package comprising:

a substrate for mounting the semiconductor chip, the substrate having a first surface and a second surface;

first to fourth groups of terminals formed on the first surface of the substrate;

first to fourth groups of wiring patterns formed on the substrate and connected to the first to fourth groups of terminals; and

fifth to eighth groups of wiring patterns formed on the second surface of the substrate and having first ends and second ends, the first ends being connected to the first to fourth groups of wiring patterns, and the second ends being parallel in each group.

5. A package according to Claim 4, wherein the fifth to eighth groups of wiring patterns are formed in first to fourth trapezoidal areas, the shorter bases of which face a center of the substrate and the longer bases of which face sides of the substrate, and the second ends of the fifth to eighth groups of wiring patterns

are along the shorter bases of the first to fourth trapezoidal areas.

6. A method for manufacturing a semiconductor device including a package having a substrate for mounting the semiconductor chip, the substrate having a first surface and a second surface; first to fourth groups of terminals formed on the first surface of the substrate; first to fourth groups of wiring patterns formed on the substrate and connected to the first to fourth groups of terminals; and fifth to eighth groups of wiring patterns formed on the second surface of the substrate and having first ends and second ends, the first ends being connected to the first to fourth groups of wiring patterns, and the second ends being parallel in each group, the method comprising the steps of:

(a) cutting the fifth to eighth groups of wiring patterns according to the size of the semiconductor chip to be packaged;

(b) mounting the semiconductor chip on the substrate;

(c) bonding the fifth to eighth groups of wiring patterns and the semiconductor chip with a plurality of wires; and

(d) encapsulating the second surface of the package and the semiconductor chip.